SEE Tolerant Self-Calibrating Simple Fractional-N PLL

Robert L. Shuler, Avionic Systems Division, NASA Johnson Space Center, Houston, TX 77058
Li Chen, Department of Electrical Engineering, University of Saskatchewan, Saskatoon, SK Canada

ABSTRACT
We show a reliable on-chip clock multiplier for SEE testing or RHBD applications. Fine control of clock frequency is provided without complex delta-sigma schemes. Conflicts that can occur with voted PLLs are discussed, and how to avoid them.

SUMMARY
Redundant VCOs can be synchronized through voting, but this leaves other sources of error. The divider can be made SEU resistant by redundancy and voting. The PFD is an asynchronous digital circuit. It can be duplicated, and possibly voted, but errors are more likely from direct hits in the charge pump, which is usually a larger area circuit. No method of voting a charge pump has been described. Suppose that the VCO and divider are separately made redundant and voted. Then errors may arise in the PFD, charge pump, or loop filter. The solution is to vote only the output of a triple redundant PLL, and avoid voting anything within the feedback loop since internal voters would hide errors from the PLL feedback correction loop. When an error occurs, we rely on the PLL feedback mechanism to re-synchronize the failed PLL with the reference clock. A diagram of this approach is shown in Figure 1.

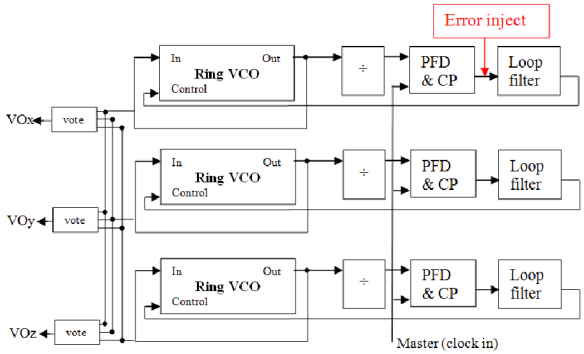

Fig. 1: Output Voted Redundant PLL (outputs on left)

To conveniently generate multiple closely spaced output frequencies, a fractional-N divider is needed, which requires compensation. Current compensation can be hard to calibrate. Delta-Sigma schemes are complex and present a large cross section to SEE. Delay based schemes are very straightforward. Since we use variable delay elements already in the VCO (current-starved inverters), we present a self-calibrating delay based compensation that appears to be novel.

An integer-N clock multiplier PLL with a range of 1x to 8x was fabricated using the TSMC .35um process. The circuit uses an auxiliary charge pump to inject an error current in one PLL of the redundant set. The output of the PLL was used to drive redundant digital logic on the same chip which was designed to detect differences in logic states, and none were detected.

We present the design and simulation of the fractional-N version, which has been submitted for fabrication in the TSMC 90nm process. It's possible results from this chip may be available in time for the symposium.